Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: EC 206

Course Name: COMPUTER ORGANIZATION

Max. Marks: 100 Duration: 3 Hours

PART A (MODULE I & II)

Answer any two out of three questions Marks

1	(a)	How is Carry- Look ahead Adder different from Ripple Carry Adder? Explain with relevant diagrams and write down the delay equations for both adders.	(10)
	b	In a 32- bit Adder circuit assume each 2 -input gate delay is 200ps. Calculate (a) Total delay for a Carry Look Ahead adder when the full adder delay is 400ps and is divided in to 4 bits block (b) Total delay for a Prefix Adder.	(5)
2	a	Design a 16-bit prefix adder and explain its working. Also obtain the delay of an N-bit prefix adder	(10)
	b	What is meant by R-Type instruction? Draw the R-Type machine instruction format. Find the machine code for the R-Type instruction add ***$s0,$s1,$s2*** with function code 32.	(5)
3	a	Design a 4-bit right and left shifter using multiplexers.	(5)
	b	What are I-Type instructions ? Explain with its instruction format.	(5)
	c	Explain the MIPS assembly codes for conditional branch instructions ***beq*** and ***bne*** with examples.	(5)

PART B (MODULE III&IV)

Answer any two out of three questions.

4	a	Discuss the different MIPS addressing modes.	(8)
	b	What are Pseudo instructions? Given the pseudo instruction " mov $s1,$s2 ". Write down its corresponding MIPS instruction and explain its working.	(7)
5	a	Describe step by step the working of a single cycle data path for subtracting two numbers.	(10)
	b	What are the parameters used for the performance analysis of a single cycle processor? Explain.	(5)

6	a	Draw and explain the working of complete MIPS multi cycle processor using an example.	(10)
	b	What are the steps involved in translating a high level language program into a machine language program ?	(5)

PART C(MODULE V&VI)

Answer any two out of three questions. Each carries 20 marks

7	a	A program has 2000 data access instructions (loads or stores), and 1250 of these requested data values are found in the cache. The other 750 data values are supplied to the processor by main memory or disk memory. What are the miss and hit rates for the cache?	(5)
	b	What is virtual memory ? Explain the process of address translation.	(5)
	c	Differentiate between programmed I/O and interrupt driven I/O.	(5)
	d	How is SRAM different from DRAM?	(5)
8	a	Explain the principle of Cache memory. What are the different cache mapping techniques? Discuss in detail.	(10)
	b	What is page table and how is it useful in address translation?	(5)
	c	Explain DMA.	(5)
9	a	Why standardisation of input/output interfaces is necessary? Explain PCI, SCSI and USB.	(8)
	b	Explain the memory system hierarchy. Draw and explain the internal organization of a memory chip.	(7)
	c	What are the various write policies used in cache?	(5)

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