



equations

- b) Consider the design of a three level memory hierarchy with the following specifications for memory characteristics:

Memory level	Access time	Capacity	Cost/Kbyte
Cache	$t_1=25$ ns	$s_1=512$ Kbytes	$c_1=\$1.25$
Main Memory	$t_2=903$ ns	$s_2=32$ Mbytes	$c_2=\$0.2$
Disk array	$t_3=4$ ms	$s_3=39.8$ Gbytes	$c_3=\$0.0002$

Hit ratio of cache memory is  $h_1=0.98$  and a hit ratio of main memory is  $h_2=0.9$ .

- (i) Calculate the effective access time.
- (ii) Calculate the total memory cost. (6)
- 13 a) Explain the role of compilers in exploiting parallelism (3)
- b) Explain VLIW architecture. Also explain pipelining in VLIW processors. (6)

### PART C

*Answer any two full questions, each carries 9 marks.*

- 14 a) Draw the state transition graph for a cache block using Goodman's write-once protocol for cache coherence. (3)
- b) Design an 8 input omega network using 2X2 switches as building blocks. (6)  
Show the switch settings for the permutation  $\pi_1=(0,6,4,7,3)(1,5)(2)$ . Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context.
- 15 a) Differentiate between synchronous and asynchronous model of linear pipeline processors. (3)
- b) Consider the following pipeline reservation table:

	1	2	3	4
S1	X			X
S2		X		
S3			X	

- i) What are the forbidden latencies?
- ii) Draw the transition diagram.
- iii) List all the simple cycles and greedy cycles.
- iv) Determine the optimal constant latency cycle and minimal average latency (MAL)

- v) Let the pipeline clock period be  $\tau=20\text{ns}$ . Determine the throughput of the pipeline. (6)
- 16 a) Explain full-map directory based protocol. (4)
- b) What do you mean by dimension order routing? Consider a 16 node hypercube network. Based on E-cube routing algorithm, show how to route a message from 0010 to 1001. Find all intermediate nodes on routing path. (5)

**PART D**

*Answer any two full questions, each carries 12 marks.*

- 17 (a) Explain the Tomasulo's algorithm for the dynamic instruction scheduling. (5)
- (b) Explain the concept of in-order issue and out-of-order issue with respect to superscalar processor. (7)
- 18 a) Explain any three latency hiding techniques used in distributed shared memory multi computers. (9)
- b) Write a short note on fine-grain parallelism. (3)
- 19 a) Explain static branch prediction strategy and dynamic branch prediction strategy. (6)
- b) With a neat diagram explain the architecture of ETL/EM-4 dataflow architecture. (6)

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